Digital Current Sharing Method for Parallel Interleaved DC-DC Converters using Input Ripple Voltage

Suyong Chae, Member, IEEE, Yujin Song, Member, IEEE, Sukin Park, Member, IEEE, and Hakgeun Jeong

Abstract—This paper describes a new digital current sharing method for parallel interleaved dc-dc converters. The difference between sensed inductor current values can cause unequal current distribution in the parallel dc-dc converters even though they are controlled by the same average current mode controller with a common current reference. To overcome this problem, a simple digital current sharing algorithm using input voltage ripple difference is proposed. The digital current sharing algorithm calculates the required current reference adjustment value using only the input ripple voltage difference information. No additional input current sensing circuit is required. The proposed algorithm achieves equal current distribution between phases of the parallel converters with high parameter insensitivity. For the experimental verification, a 500W two phase interleaved synchronous buck dc-dc converter which charges a 24V Li-ion battery is implemented.

Index Terms—Current sharing, Digital control, Minimum point tracking, Parallel dc-dc converters, Ripple voltage.

I. INTRODUCTION

The application area of the direct current based renewable energy source like fuel cell or photovoltaic panel is spreading widely from large scale power generation plant to small size compact power source. The increasing power capacity of the renewable energy source requires an interfaced power management system to process large amount of direct current effectively. The power management system should use a dc-dc converter as a power processing unit to provide a regulated dc voltage for the target application.

The one of the important roles of the dc-dc converter applied in this application is to stabilize the power generation capability of the renewable energy source by using the energy storage unit. The hybrid power system [1]-[8] combined with a rechargeable secondary battery shows fast dynamic response and high reliability by compensating output power characteristics of the renewable energy source. The parallel interleaved dc-dc converter applied in this hybrid power system has many advantages as it can provide sufficient output current and reduced output voltage ripple with high efficiency [9]-[11].

The dc-dc converter for the battery charging purpose should regulate the output current precisely in accordance with the battery voltage and SOC [12], [13] status. The average current mode control is an appropriate control method for precise adjustment of the battery charging current depending on a current reference command. Additionally, the current sharing among converter phases can be easily achieved by the average current mode control [14]-[16]. The disadvantage of this control method is that the current control accuracy is highly affected by the inductor current sensing circuitry. So, the difference in the sensed current value can cause the unequal current distribution between phases of the parallel converters. The large ripple current induced by the unequal current distribution has a negative effect on the battery’s lifetime [17], [18]. To overcome the dependency on the sensing accuracy, some current sharing methods [19]-[26] have been introduced.

The duty cycle matching method [19]-[22] normally focuses on the efficacy improvement of parallel dc-dc converters. The previous methods show efficient current distribution between the parallel converters without the current sensing problem. However, these methods are not adequate for the battery charging purpose, as it could not control the charging current precisely. In some case, the equal current distribution between the converters may not be guaranteed because of the gate drivers’ differences or parasitic resistances.

The digital current sharing method has been used to achieve the equal current distribution effectively [23]-[26]. The digital control method in [23] used a single current sensor, but the current sensing was based on the additional active switches. The digital current unbalance measurement method between parallel converters without an additional current sensing circuit was introduced in [26]. However, this method requires a complex computational algorithm.

This paper introduces a simple digital current sharing method based on the minimum difference point tracking algorithm using the input ripple voltage. The difference value of the common input voltage ripple is used as a measure to detect the current sharing status of the interleaved parallel dc-dc converters. The proposed digital control algorithm calculates the required current reference value for the equal current distribution using a simple perturbation and observation method.

This paper is organized as follows. Section II explains the proposed digital control method including the basic operational principle. The small signal model and the performance analysis are introduced in Section III. Section IV presents the actual test
results of a prototype 500W two phase interleaved synchronous buck dc-dc converter which charges a 24V Li-ion battery. The conclusion will be presented in the final section.

II. CONTROL METHOD AND INPUT VOLTAGE RIPPLE

A. System Configuration

Fig. 1 shows the two phase interleaved synchronous buck dc-dc converter with the proposed control scheme, which includes the digital controller, the input ripple voltage detection circuit and the analog average current mode controller.

The dc-dc converter is comprised of two modules. Each module contains an analog average current mode controller to provide precisely regulated battery charging current designated by the current reference signal, $i_{\text{ref1}}$ or $i_{\text{ref2}}$. The inductor currents, $i_{L1}$ and $i_{L2}$, are sensed using the series resistors, $r_{s1}$ and $r_{s2}$, and the sensed values are compared with the current reference signals in the analog average current mode controller.

If $r_{s1}$ and $r_{s2}$ are unequal due to the different aging process by time or temperature, the current distribution ratio between two modules will be different even though they are controlled to follow a common current reference signal.

In order to solve this problem, the proposed digital minimum ripple voltage difference tracking algorithm calculates the required current reference adjustment values, $\Delta i_{L1}$ and $\Delta i_{L2}$, by using the ripple voltage of the input capacitor. The ripple voltage, $v_{\text{in}_{-rf}}$, is obtained by the input ripple voltage detection circuit. The detection circuit is comprised of the differential amplifier, resistor-capacitor network and low pass filter (LPF). The dc component and switching noise of the input voltage are removed through this detection circuit.

The ripple voltage is digitized by an analog-to-digital converter (ADC) in the digital controller. The minimum ripple voltage difference tracking (MRDT) controller finds a minimum point of the input ripple voltage difference using a simple perturbation and observation method which is widely used in the photovoltaic power conditioning system applications [27]. The MRDT controller changes the current reference adjustment values, $\Delta i_{L1}$ and $\Delta i_{L2}$, and monitors the low pass filtered input ripple voltage to decide whether the difference is minimum or not. If the controller reaches at a minimum point, it stops to change the current reference adjustment values.

The common current reference signal, $i_{\text{ref}}$, for charging the battery is generated using the information transmitted from the battery management system (BMS) and the sensed voltage level, $v_b$, of the battery. The sync signals, $\text{sync}_{1}$ and $\text{sync}_{2}$, with 180° phase difference are provided to the PWM generator of each module for the interleaving operation.

B. Inductor current and Input ripple voltage

The key current and voltage waveforms during a switching period, $T_s$, are shown in Fig. 2. It is assumed that the duty ratios, $d_1$ and $d_2$, are greater than 0.5 as well as followings: (a) all active switches are ideal; (b) switching periods of the two modules are equal; (c) duty ratios of the two modules are equal($d_1=d_2=d$); (d) $r_{s1}$ and $r_{s2}$ are very small not to affect the duty ratio; (e) $L_1$ and $L_2$ are equal; (f) $v_{\text{in}}$, $v_b$, and $i_{\text{ref}}$ are constant during a switching period; (g) $i_{\text{ref1}}$ and $i_{\text{ref2}}$ are equal.

If $r_{s2}$ is smaller than $r_{s1}$, the inductor current of the 2nd module, $i_{L2}$, flows higher than the inductor current of the 1st module, $i_{L1}$, as shown in Fig. 2(a). If $r_{s2}$ is greater than $r_{s1}$, the inductor current of the 2nd module, $i_{L2}$, flows lower than the inductor
current of the 1st module, \(i_{L1}\), as shown in Fig. 2(b). The inductor current difference, \(\Delta i_L\), is defined as

\[
\Delta i_L = \frac{1}{T_s} \int_0^T i_{L2}(t) dt - \frac{1}{T_s} \int_0^T i_{L1}(t) dt = I_{L2} - I_{L1}
\]

(1)

where \(I_{L2}\) is the average value of \(i_{L2}\) and \(I_{L1}\) is the average value of \(i_{L1}\). The rising slope, \(s_r\), of the inductor currents is

\[
s_r = \frac{v_{in}}{L_1} = \frac{v_{in}}{L_2}.
\]

(2)

The input voltage source output current, \(i_{sc}\), is equal to the average value of the input current, \(i_in\). From (1) and (2), \(i_{in}\) is expressed as

\[
i_{in} = \frac{1}{T_s} \int_0^T i_{in}(t) dt = \left(2i_{s1} + \Delta i_L + s_r dT_s\right) d.
\]

(3)

The peak input capacitor current during the first half of a switching period, \(i_{ci,p1}\), is

\[
i_{ci,p1} = i_{sc} - \left(i_{s1} + s_r (d - 0.5)T_s + \Delta i_L\right)
\]

\[
= (2d-1)i_{s1} + \left(d^2 - d + 0.5\right)s_r T_s + (d-1)\Delta i_L.
\]

(4)

The peak input capacitor current during the second half of a switching period, \(i_{ci,p2}\), is

\[
i_{ci,p2} = i_{sc} - \left(i_{s1} + s_r (d - 0.5)T_s + \Delta i_L\right)
\]

\[
= (2d-1)i_{s1} + \left(d^2 - d + 0.5\right)s_r T_s + (d-1)\Delta i_L.
\]

(5)

From (4) and (5), the peak capacitor current difference, \(\Delta i_{ci,p}\), is expressed as

\[
\Delta i_{ci,p} = i_{ci,p1} - i_{ci,p2} = \Delta i_L.
\]

(6)

The peak input ripple voltage, \(v_{in,rp1}\), during the first half of a switching period is

\[
v_{in,rp1} = r_c i_{ci,p1} + \frac{1}{C_i} \left[\int_{t=0}^{T_s} i_{ci}(t) dt\right] + \frac{1}{C_i} \left[0^{(0.5)}{r_c} i_{ci}(t) dt\right].
\]

(7)

The peak input ripple voltage, \(v_{in,rp2}\), during the second half of a switching period is

\[
v_{in,rp2} = r_c i_{ci,p2} + \frac{1}{C_i} \left[\int_{t=0}^{T_s} i_{ci}(t) dt\right] + \frac{1}{C_i} \left[0^{(0.5)}{r_c} i_{ci}(t) dt\right].
\]

(8)

From (6) to (8), the peak input ripple voltage difference, \(\Delta v_{in,rp}\), is expressed as

\[
\Delta v_{in,rp} = v_{in,rp1} - v_{in,rp2} = \left(r_c + \frac{1-d}{2C_i} T_s\right) \Delta i_L.
\]

(9)

where \(r_c\) is the equivalent series resistance(ESR) of the input capacitor, \(C_i\). The peak input voltage ripple difference is linearly proportional to the inductor current difference. It means that the absolute value of the peak input voltage ripple difference goes to the minimum point\((\Delta v_{in,rp}=0)\) when the inductor currents are equally distributed\((\Delta i_L=0)\) between two modules.

The digital controller digitizes the input ripple voltage using the ADC. To detect the input ripple voltage difference properly, the input capacitor should be selected carefully as the magnitude of the ripple voltage difference is highly affected by the ESR. From (9), the minimum required ESR of the input capacitor is defined as

\[
r_{ci,min} > \frac{\Delta v_{per}}{K_{LPF} \Delta i_{ci,min}} - \frac{1-d}{2C_i} T_s
\]

(10)

where \(K_{LPF}\) is the LPF gain of the input ripple voltage detection circuit at the switching frequency. In (10), \(\Delta v_{per}\) is the minimum detectable voltage difference of the ADC and \(\Delta i_{ci,min}\) is the minimum allowed inductor current difference.

Fig. 3 shows the calculated and measured absolute value of the peak input ripple voltage difference. The voltage difference calculation is executed using the same parameters that are used in the experiment. It is shown in Fig. 3 that the measured value
matches calculated one within 12mV. From (9) and Fig. 3, we can see that if we find out a minimum difference point, the exact current distribution between two modules can be achieved.

C. Minimum Ripple Voltage Difference Tracking (MRDT) algorithm

The proposed minimum ripple voltage difference tracking algorithm flowchart is shown in Fig. 4. The low pass filtered input ripple voltage, $v_{in, rf}$, is sampled once during a switching period, $T_s$, with 180° phase difference. The sampled ripple voltages are $v_{in, rf}[k]$ and $v_{in, rf}[k]$. The $\Delta v_{in, rf}[n]$ is calculated at every ‘m’ times switching periods using the average values. And the absolute value of the difference, $|\Delta v_{in, rf}[n]|$, is compared with a threshold voltage, $v_{rp, th}$, to determine whether the voltage difference is small enough to guarantee equal current distribution between two modules.

The algorithm changes only the current reference of a module that shows higher inductor current than the other one. The current reference decrement step is $i_{r, step}$. The current adjustment values, $\Delta i_1[n]$ and $\Delta i_2[n]$, are added to the common current reference signal, $i_{ref}[n]$. The current reference signals of each module are defined as follows.

$$i_{ref_1}[n] = i_{ref}[n] + \Delta i_1[n],$$
$$i_{ref_2}[n] = i_{ref}[n] + \Delta i_2[n].$$

The algorithm continues operation until $|\Delta v_{in, rf}[n]|$ is smaller than a threshold voltage, $v_{rp, th}$. The algorithm stops to decrease the current reference adjustment value if it finds out a minimum voltage difference point. The algorithm restarts when $|\Delta v_{in, rf}[n]|$ is greater than $v_{rp, th}$.

The proposed algorithm can be expanded for a dc-dc converter with higher number of phases. In this case, the peak input ripple voltage variance, $S_{viu, rp}$, is used as a measure to detect the current sharing status between parallel modules. From (7) to (9), the peak input ripple voltage variance is defined as

$$S_{viu, rp} = \frac{1}{P} \sum_{i=1}^{P} \left( v_{in, rp,i} - \bar{v}_{in, rp} \right)^2$$

where $P$ is the number of parallel modules and $\bar{v}_{in, rp}$ is the average value of the sampled input ripple voltage points in a switching period.

Fig. 5 shows the simulated peak input ripple voltage variance of a three phase synchronous buck converter. It is shown in Fig. 5 that the variance goes to a minimum point when inductor currents are equally distributed between the three phase modules. The algorithm flowchart of Fig. 4 can be used by substituting the ripple voltage difference, $\Delta v_{in, rf}$, into the ripple voltage variance, $S_{viu, rp}$. The algorithm is applied at two modules at a time in a sequential manner until it finds out a minimum variance point.
III. SMALL SIGNAL MODELING AND ANALYSIS

A. Small Signal Modeling

The stability and performance of the proposed control method are analyzed by means of a small signal model. If we consider a state space averaging method and a small perturbation from its steady state value,

\[
\begin{align*}
\hat{d}_1 &= D_1 + \hat{d}_1, \\
\hat{d}_2 &= D_2 + \hat{d}_2, \\
i_{11} &= I_{11} + \hat{i}_{11}, \\
i_{12} &= I_{12} + \hat{i}_{12}, \\
i_{\text{ref}} &= I_{\text{ref}} + \hat{i}_{\text{ref}}, \\
i_{\text{ref}1} &= I_{\text{ref}1} + \hat{i}_{\text{ref}1}, \\
i_{\text{ref}2} &= I_{\text{ref}2} + \hat{i}_{\text{ref}2}, \\
v_{\text{in}} &= V_{\text{in}} + \hat{v}_{\text{in}},
\end{align*}
\]

the open loop small signal model of the two phase synchronous buck converter in Fig. 1 can be calculated as follows:

\[
\begin{align*}
G_{a11}(s) &= \frac{i_{11}}{d_1} = \frac{r_2 + sL_2}{2(r_1 + r_2) + s(L_1 + L_2)} + \frac{v_{\text{in}}C_1}{\Delta_s}, \\
G_{a12}(s) &= \frac{i_{11}}{d_1} = \frac{r_2 + sL_2}{2(r_1 + r_2) + s(L_1 + L_2)} + \frac{v_{\text{in}}C_1}{\Delta_s}, \\
G_{a21}(s) &= \frac{i_{22}}{d_2} = \frac{r_2 + sL_2}{2(r_1 + r_2) + s(L_1 + L_2)} + \frac{v_{\text{in}}C_1}{\Delta_s}, \\
G_{a22}(s) &= \frac{i_{22}}{d_2} = \frac{r_2 + sL_2}{2(r_1 + r_2) + s(L_1 + L_2)} + \frac{v_{\text{in}}C_1}{\Delta_s},
\end{align*}
\]

where

\[
\Delta_s = 1 + \frac{s}{Q_{\text{in}}w_c + s^2} + \frac{s^2}{w_0^2}, \quad w_c = \frac{1}{\sqrt{L_2C}}, \quad Q = \frac{1}{r_1 \sqrt{L_2/C}}, \\
r_i = \frac{r_i + r_{i2}}{r_1 + r_2}, \quad L_{i1} = \frac{L_1L_2}{L_1 + L_2}.
\]

The \(G_{a11}(s)\) and \(G_{a22}(s)\) are transfer functions representing the inductor current behavior according to the duty cycle variation of each module. The \(G_{a12}(s)\) and \(G_{a21}(s)\) are transfer functions representing interactions between the two converter modules.

The small signal block diagram including the analog average current mode compensator [28], \(G_s(s)\) and \(G_p(s)\), is depicted in Fig. 6. In Fig. 6, \(H_s(s)\) represents sampling effect of the current loop and \(K_a\) is a gain of the differential amp. The modulator gain is \(F_m\). The current loop gains, \(T_{i1}(s)\) and \(T_{i2}(s)\), are expressed as follows:

\[
\begin{align*}
T_{i1}(s) &= F_mH_s(s)\frac{r_iK_sG_s(s)G_{a11}(s)}{1 + T_i(s)}, \\
T_{i2}(s) &= F_mH_s(s)\frac{r_iK_sG_s(s)G_{a12}(s)}{1 + T_i(s)}.
\end{align*}
\]

The designed current loop gains with parameters used in the experimental prototype are shown in Fig. 7. The bandwidth of the loop gain, \(f_{\text{ci}}\), is designed greater than 10kHz for the inductor current to follow the current reference signal of each module correctly.

B. Performance Analysis

The current sharing performance of the proposed digital control algorithm is analyzed using the common current reference to inductor current transfer functions. From Fig. 6, the transfer functions are defined as following equations when the proposed digital controller is not applied.

\[
\begin{align*}
G_{a11}(s) &= \frac{\hat{i}_{11}}{i_{\text{ref}1}} = \frac{\hat{i}_{11}}{i_{\text{ref}1}} \approx \frac{F_mG_s(s)G_{a11}(s)}{1 + T_i(s)},
\end{align*}
\]
Fig. 8. Common current reference to inductor current transfer functions without the proposed algorithm

\[
G_{ir11}(s) = \frac{F_m G_i (s) G_p (s) G_{d22}(s)}{1 + T_i (s)}.
\]  

(15)

The \( G_{ir11}(s) \) and \( G_{ir22}(s) \) with parameters used in the experimental prototype are shown in Fig. 8. It is observed in Fig. 8 that the inductor currents, \( i_{L1} \) and \( i_{L2} \), follow the common current reference signal, \( i_{ref} \), up to 100Hz without large magnitude or phase distortion. The frequency sweep simulation results are matched with the calculation results. However, the low frequency magnitudes of \( G_{ir11}(s) \) and \( G_{ir22}(s) \) are different by 1.94dB because of the unequal current sensing resistors \((r_{s1}=5m\Omega, r_{s2}=4.2m\Omega)\). This magnitude difference causes an unequal current distribution between modules when a common current reference is used.

The common current reference to inductor current transfer functions with the proposed digital controller are represented as

\[
G_{ir1c}(s) = \frac{i_{L1}}{i_{ref}} = K_{ref1} G_{soh}(s) G_{r11}(s),
\]

\[
G_{ir2c}(s) = \frac{i_{L2}}{i_{ref}} = K_{ref2} G_{soh}(s) G_{r22}(s)
\]

where

\[
K_{ref1} = \left(1 + \frac{\Delta i_{r1}}{i_{ref}}\right), \quad K_{ref2} = \left(1 + \frac{\Delta i_{r2}}{i_{ref}}\right),
\]

\[
G_{soh}(s) = \frac{1 - e^{-sT_i}}{sT_i}.
\]  

(16)

The current reference adjustment gains, \( K_{ref1} \) and \( K_{ref2} \), are calculated from the proposed digital MRDT controller. If we assume that the MRDT controller finds out a zero ripple voltage difference point and \( r_{s1} \) is greater than \( r_{s2} \), the calculated \( K_{ref1} \) and \( K_{ref2} \) from the MRDT controller are equal to following values: \( K_{ref1}=1 \), \( K_{ref2}=r_{s2}/r_{s1} \). These different current reference adjustment gains make the \( G_{ir1c}(s) \) and \( G_{ir2c}(s) \) have the same low frequency magnitudes even though the current sensing resistors are different. The same low frequency magnitudes result in an equal current distribution between modules with a common current reference.

In order to examine the influence of the MRDT controller, the \( G_{ir1c}(s) \) and \( G_{ir2c}(s) \) are plotted using parameters that are used in the experiment. It is observed in Fig. 9 that the MRDT controller makes the magnitudes of the transfer functions equal up to 100Hz. The frequency sweep simulation results are matched with the calculation results. The equal current distribution between modules can be achieved using the MRDT controller. The update frequency of the adjustment gains, \( f_{mrdt} \), is set as 100Hz to guarantee correct reference following performance. The MRDT controller does not affect the current loop stability as \( f_{ci} \) is 100 times greater than \( f_{mrdt} \).

The parameter sensitivity analysis to the current sensing resistor difference is executed using the following sensitivity function.

\[
\Delta i_L = f_{ai} (\Delta r_i)
\]  

(17)

where \( \Delta i_{L}=i_{L1}-i_{L2} \) and \( \Delta r_i=r_{s1}-r_{s2} \). The sensitivity function is simulated using the PSIM®. The simulation results are shown in Fig. 10. From Fig. 10, it can be noticed that the variation of \( f_{ai} \) is decreased by 88% after applying the proposed algorithm. It means that the converter with the proposed algorithm achieves high parameter insensitivity in comparison to the converter without the proposed algorithm.

IV. EXPERIMENTAL RESULTS

To demonstrate the performance of the proposed digital current sharing algorithm, a 500W prototype two phase interleaved synchronous buck dc-dc converter which charge a 24V(20Ah) Li-ion battery with a constant current mode [29] was implemented. The key converter parameters are listed in Table I.

The analog average current controller of each module is
Table I

<table>
<thead>
<tr>
<th>Converter Parameters</th>
<th>Power stage</th>
<th>Controller</th>
</tr>
</thead>
<tbody>
<tr>
<td>(v_{in})</td>
<td>Input voltage range</td>
<td>(F_s)</td>
</tr>
<tr>
<td>(v_{in_nom})</td>
<td>Nominal input voltage range</td>
<td>(T_s)</td>
</tr>
<tr>
<td>(v_{o})</td>
<td>Output voltage</td>
<td>(K_a)</td>
</tr>
<tr>
<td>(C_i)</td>
<td>Input capacitance</td>
<td>(56\mu F \times 3)</td>
</tr>
<tr>
<td>(r_{ci})</td>
<td>Input capacitor ESR</td>
<td>(90m\Omega / 3)</td>
</tr>
<tr>
<td>(C_o)</td>
<td>Output capacitance</td>
<td>(33\mu F \times 5)</td>
</tr>
<tr>
<td>(r_{co})</td>
<td>Output capacitor ESR</td>
<td>(100m\Omega / 5)</td>
</tr>
<tr>
<td>(L_1)</td>
<td>Inductance of 1st module</td>
<td>10\mu H</td>
</tr>
<tr>
<td>(L_2)</td>
<td>Inductance of 2nd module</td>
<td>10\mu H</td>
</tr>
<tr>
<td>(r_{s1})</td>
<td>Current sensing resistance of 1st module</td>
<td>5m\Omega</td>
</tr>
<tr>
<td>(r_{s2})</td>
<td>Current sensing resistance of 2nd module</td>
<td>4.2m\Omega</td>
</tr>
</tbody>
</table>

**designed to have a bandwidth greater than 10kHz. The phase margins are greater than 45°. The bandwidth is designed high enough to follow the current reference signal of each module correctly. The update period of the reference adjustment signal is set to 10ms in the digital controller. The proposed digital controller is implemented using a TI’s digital signal processor (TMS320F28335).**

Fig. 11 and Fig. 12 show the experimental result when the converter operates without the current sharing algorithm. The common current reference, \(i_{ref}\), is 5A and the sensing resistors are equal \((r_{s1} = r_{s2} = 5m\Omega)\). The signal marked as \(v_{in\_rf}\) is a 300kHz low pass filtered input ripple voltage signal. This signal is sampled and processed in the digital controller to detect the ripple voltage difference. It is observed in Fig. 11 that the inductor currents are equally distributed and the peak values of the input ripple voltage are equal. Fig. 12 shows the experimental result at \(i_{ref} = 5A\) and \(r_{s1} > r_{s2}\) \((r_{s1} = 5m\Omega, r_{s2} = 4.2m\Omega)\). As \(r_{s2}\) is smaller than \(r_{s1}\) by 23%, the inductor current of the 2nd module is higher than the inductor current of the 1st module by 1.5A. The filtered input ripple voltage difference is about 40mV. From Fig. 11 and Fig. 12, it can be noticed that the peak input voltage ripple difference is a measure to detect current distribution ratio between two modules.

It is shown in Fig. 13 that the proposed digital control algorithm achieves equal current distribution even though the current sensing resistors are unequal. The experimental condition
is as follows: $v_{in}=35V$, $i_{ref}=8A$, $r_{s1}=5m\Omega$, $r_{s2}=4.2m\Omega$. Before point A, $i_{L1}$ is greater than $i_{L2}$ by 1.5A. The algorithm starts at point A. The current reference of the 2nd module, $i_{ref2}$, changes from 3.65V to 3.53V until $i_{L1}$ and $i_{L2}$ are equally distributed. The current reference goes to the steady state in 300ms.

Fig. 14 shows a closer look near point A of Fig. 13. The current reference changes at every 10ms and the decrement step is 20mV. Fig. 15 is detailed waveforms before the algorithm is applied. The detailed waveforms after applying the proposed algorithm are shown in Fig. 16. It is shown in Fig. 16 that inductor currents are equally distributed by decreasing the current reference of the 2nd module.

The experimental results with different input voltage conditions are shown in Fig. 17 and Fig. 18. From Fig. 17 and Fig. 18, it is observed that the proposed algorithm operates properly under various input voltage conditions.

V. Conclusion

This paper introduces a new digital current sharing method for parallel interleaved dc-dc converters with high sensing parameter insensitivity, which utilizes the input ripple voltage difference information. The proposed digital current sharing algorithm achieves equal current distribution between modules by finding out an absolute minimum ripple voltage difference point using the perturbation and observation method. No additional input current sensing circuit is required. The experimental results show that the inductor currents are equally distributed even though the current sensing resistors are unequal. Test results are obtained with a 500W two phase interleaved synchronous buck dc-dc converter.
REFERENCES


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